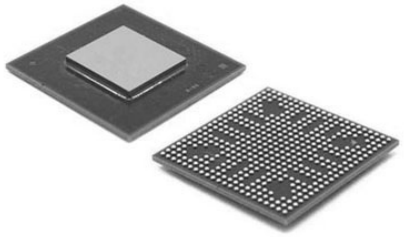
AD9514BCPZ

Data Sheet

Clock Distribution, 1.6 GHz, 3.135V-3.465V supply, 3 Outputs, LFCSP-32

Manufacturers	Analog Devices, Inc
Package/Case	LFCSP-32
Product Type	Clock & Timer ICs
RoHS	Pb-free Halide free
Lifecycle	



Images are for reference only

Please submit RFQ for AD9514BCPZ or Email to us: sales@ovaga.com We will contact you in 12 hours. RFQ

General Description

There are three independent clock outputs. Two of the outputs are LVPECL, and the third output can be set to either LVDS or CMOS levels. The LVPECL outputs operate to 1.6 GHz, and the third output operates to 800 MHz in LVDS mode and to 250 MHz in CMOS mode.

Each output has a programmable divider, which can be set to divide by a selected set of integers ranging from 1 to 32. The phase of one clock output relative to another clock output can be set by means of a divider phase select function that serves as a coarse timing adjustment.

The LVDS/CMOS output features a delay element with three selectable full-scale delay values (1.5 ns, 5 ns, and 10 ns), each with 16 steps of fine adjustment.

The AD9514 does not require an external controller for operation or setup. The device is programmed by means of 11 pins (S0 to S10) using 4-level logic. The programming pins are internally biased to ⅓ VS. The VREF pin provides a level of ⅔ VS. VS (3.3 V) and GND (0 V) provide the other two logic levels.

The AD9514 is ideally suited for data converter clocking applications where maximum converter performance is achieved by encode signals with subpicosecond jitter.

The AD9514 is available in a 32-lead LFCSP and operates from a single 3.3 V supply. The temperature range is −40°C to +85°C.

Features

1.6 GHz differential clock input

3 programmable dividers, in range from 1 to 32Phase select for output-to-output coarse delay adjust

2 independent 1.6 GHz LVPECL clock outputs LVPECL Additive broadband output jitter 225 fs rms

1 independent 800 MHz/250 MHz LVDS/CMOS clock outputLVDS/CMOS Additive broadband output jitter 300 fs rms/290 fs rmsTime delays up to 10 ns

Device configured with 4-level logic pins

Space-saving, 32-lead LFCSP

Application

Low jitter, low phase noise clock distribution

Clocking high speed ADC, DAC, DDS, DDC, DUC, MxFE

High performance wireless transceivers

High performance instrumentation

Broadband infrastructure

ATE

Related Products

ADF4350BCPZ

Analog Devices, Inc

LFCSP-32

AD9516-4BCPZ

Analog Devices, Inc

LFCSP64

ADF4111BRUZ

Analog Devices, Inc

TSSOP-16

ADF4113BRUZ

Analog Devices, Inc

TSSOP-16

ADF4116BRUZ

Analog Devices, Inc

TSSOP-16

ADF4110BRUZ

Analog Devices, Inc

TSSOP-16

ADF4193BCPZ

Analog Devices, Inc

LFCSP-32

AD2S99BPZ

Analog Devices, Inc

PLCC-20