

AD7175-2BRUZ

Data Sheet

4-Channel Single ADC Delta-Sigma 250ksps 24-bit Serial 24-Pin TSSOP Tube

Manufacturers Analog Devices, Inc

Package/Case 24-TSSOP (0.173", 4.40mm Width)

Product Type Data Conversion ICs

RoHS Pb-free Halide free

Please submit RFQ for AD7175-2BRUZ or Email to us: sales@ovaga.com We will contact you in 12 hours.



Images are for reference only

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General Description

Lifecycle

The AD7175-2 is a low noise, fast settling, multiplexed, 2-/4-channel (fully/pseudo differential) Σ - Δ analog-to-digital converter(ADC) for low bandwidth inputs. It has a maximum channelscan rate of 50 kSPS (20 μ s) for fully settled data. The output data rates range from 5 SPS to 250 kSPS.

The AD7175-2 integrates key analog and digital signal conditioningblocks to allow users to configure an individual setup foreach analog input channel in use. Each feature can be user selected on a per channel basis. Integrated true rail-to-rail buffers on theanalog inputs and external reference inputs provide easy to drivehigh impedance inputs. The precision 2.5 V low drift (2 ppm/°C) band gap internal reference (with output reference buffer) addsembedded functionality to reduce external component count.

The digital filter allows simultaneous 50 Hz/60 Hz rejection at 27.27 SPS output data rate. The user can switch between different filter options according to the demands of each channel in the application. The ADC automatically switchesthrough each selected channel. Further digital processing functions include offset and gain calibration registers, configurable on a per channel basis.

The device operates with a 5 V AVDD1, or ± 2.5 V AVDD1/AVSS, and 2 V to 5 V AVDD2 and IOVDD supplies. The specified operating temperature range is -40° C to $\pm 105^{\circ}$ C. The AD7175-2 isin a 24-lead TSSOP package.

Features

Fast and flexible output rate: 5 SPS to 250 kSPS

Channel scan data rate of 50 kSPS/channel (20 µs settling)

Performance specifications

17.2 noise free bits at 250 kSPS

20 noise free bits at 2.5 kSPS

24 noise free bits at 20 SPS

INL: ±1 ppm of FSR

85 dB rejection of 50 Hz and 60 Hz with 50 ms settling

User configurable input channels

2 fully differential channels or 4 single-ended channels

Crosspoint multiplexer

On-chip 2.5 V reference (±2 ppm/°C drift)

True rail-to-rail analog and reference input buffers

Internal or external clock

Power supply: =>

Split supply with AVDD1/AVSS at $\pm 2.5~V$

ADC current: 8.4 mA

Temperature range: -40°C to +105°C

3- or 4-wire serial digital interface (Schmitt trigger on SCLK)

Serial port interface (SPI), QSPI, MICROWIRE, and DSP compatible

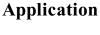
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Analog Devices, Inc
LFCSP-40



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