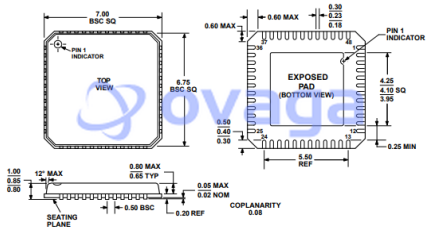
AD9233BCPZ-125

Data Sheet

Analogue to Digital Converter, 12 bit, 125 MSPS, Differential, Single Ended, Parallel, Single

Manufacturers	Analog Devices, Inc
Package/Case	LFCSP-48
Product Type	Data Conversion ICs
RoHS	Rohs
Lifecycle	



Images are for reference only

Please submit RFQ for AD9233BCPZ-125 or Email to us: sales@ovaga.com We will contact you in 12 hours. RFQ

General Description

The AD9233 is a monolithic, single 1.8 V supply, 12-bit, 80 MSPS/ 105 MSPS/125 MSPS analog-to-digital converter (ADC), featuring a high performance sample-and-hold amplifier (SHA) and on-chip voltage reference. The product uses a multistage differential pipeline architecture with output error correction logic to provide 12-bit accuracy at 125 MSPS data rates and guarantees no missing codes over the full operating temperature range.

The wide bandwidth, truly differential SHA allows a variety of user-selectable input ranges and offsets, including single-ended applications. It is suitable for multiplexed systems that switch full-scale voltage levels in successive channels and for sampling single-channel inputs at frequencies well beyond the Nyquist rate. Combined with power and cost savings over previously available ADCs, the AD9233 is suitable for applications in communications, imaging, and medical ultrasound.

A differential clock input controls all internal conversion cycles. A duty cycle stabilizer (DCS) compensates for wide variations in the clock duty cycle while maintaining excellent overall ADC performance.

The digital output data is presented in offset binary, Gray code, or twos complement formats. A data output clock (DCO) is provided to ensure proper latch timing with receiving logic.

The AD9233 is available in a 48-lead LFCSP and is specified over the industrial temperature range (−40°C to +85°C).

Product Highlights

Applications

The AD9233 operates from a single 1.8 V power supply and features a separate digital output driver supply to accommodate 1.8 V to 3.3 V logic families.

The patented SHA input maintains excellent performance for input frequencies up to 225 MHz.

The clock DCS maintains overall ADC performance over a wide range of clock pulse widths.

A standard serial port interface supports various product features and functions, such as data formatting (offset binary, twos complement, or

Gray coding), enabling the clock DCS, power-down, and voltage reference mode.

The AD9233 is pin compatible with the AD9246, allowing a simple migration from 12 bits to 14 bits.

Features

Chinese data sheet available

1.8 V analog supply operation

1.8 V to 3.3 V output supply

Low power: 395 mW @ 125 MSPS

Differential input with 650 MHz bandwidth

On-chip voltage reference and sample-and-hold amplifier

11-bit 140Msps device available (AD80141)

Flexible analog input: 1 V p-p to 2 V p-p range

Offset binary, Gray code, or twos complement data format

Data output clock and clock duty cycle stabilizer

Serial port control

Built-in selectable digital test pattern generation

Programmable clock and data alignment

Application

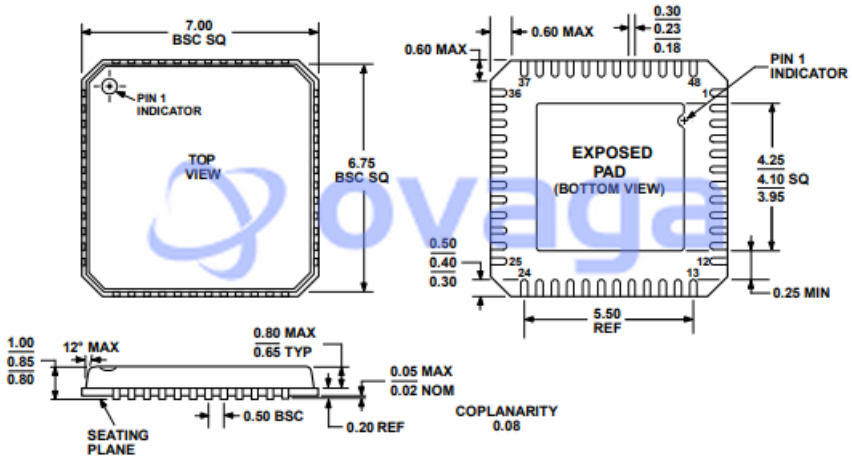
Ultrasound equipment

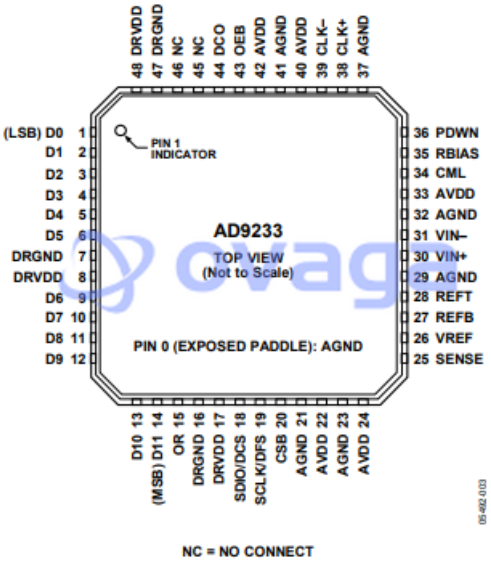
IF sampling in communications receivers

Battery-powered instruments

Hand-held scopemeters

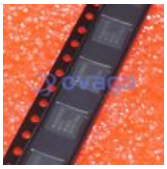
Low cost digital oscilloscopes





NC = NO CONNECT

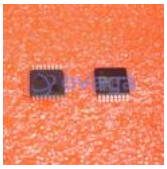
Related Products



[ADAS3022BCPZ]

Analog Devices, Inc

LFCSP-40



[AD7266BSUZ]

Analog Devices, Inc

TQPF-32

[AD574AJNZ]

Analog Devices, Inc

PDIP-28

[AD7401YRWZ]

Analog Devices, Inc

SOIC-16

[AD7938BSUZ]

Analog Devices, Inc

TQFP-32

[AD7192BRUZ-REEL]

Analog Devices, Inc

TSSOP-24

[AD7124-8BCPZ-RL7]

Analog Devices, Inc

LFCSP-32

[AD9680BCPZ-500]

Analog Devices, Inc

LFCSP-64