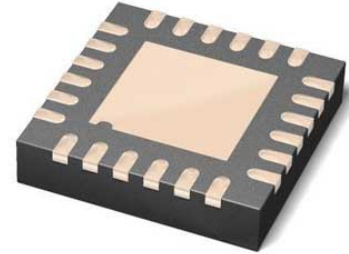


I2C/SMBus Interface 100kHz/400kHz/1000kHz 5.5V 24-Pin QFN EP T/R

|               |                                       |
|---------------|---------------------------------------|
| Manufacturers | <a href="#">ON Semiconductor, LLC</a> |
| Package/Case  | QFN-24                                |
| Product Type  | Interface ICs                         |
| RoHS          | Rohs                                  |
| Lifecycle     |                                       |



Images are for reference only

Please submit RFQ for PCA9655EMTTXG or [Email to us: sales@ovaga.com](mailto:sales@ovaga.com) We will contact you in 12 hours.

[RFQ](#)

## General Description

The PCA9655E provides 16 bits of General Purpose parallel Input and Output (GPIO) expansion through the I2C-bus and SMBus. The PCA9655E consists of two 8-bit Configuration (Input or Output selection); Input, Output and Polarity Inversion (active-HIGH) or active-LOW operation) registers. At power on, all IOs default to inputs. Each IO may be configured as either input or output by writing to its corresponding IO configuration bit. The data for each Input or Output is kept in its corresponding Input or Output register. The Polarity Inversion register may be used to invert the Polarity if the read register. All registers can be read by the system master. The PCA9655E provides an open-drain interrupt output which is activated when any input state differs from its corresponding input port register state. The interrupt output is used to indicate to the system master that an input state has changed. The power-on reset sets the registers to their default values and initializes the device state machine. Three hardware pins (AD0, AD1, AD2) are used to configure the I2C-bus slave address of the device. Up to 64 devices are allowed to share the same I2C-bus and SMBus.

## Features

VCC Operating Range: 1.65 V to 5.5 V

SDA Sink Capability: 30 mA

5.5 V Tolerant I/Os

Polarity Inversion Register

Active LOW Interrupt Output

Low Standby Current

Noise Filter on SCL/SDA Inputs

No Glitch on Powerup

Internal Power on Reset

64 Programmable Slave Addresses Using Three Address Pins

16 I/O Pins Which Default to 16 Inputs

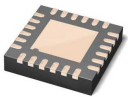
I2C SCL Clock Frequencies Supported: Standard Mode: 100 kHz/Fast Mode: 400 kHz/Fast Mode +: 1 MHz

ESD Performance: 2000 V Human Body Model, 200 V Machine Model

## Application

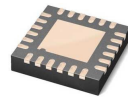
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## Related Products



### [PCA9535EMTTXG](#)

ON Semiconductor, LLC  
QFN-24



### [PCA9535ECMTTXG](#)

ON Semiconductor, LLC  
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### [PCA9654EDTR2G](#)

ON Semiconductor, LLC  
TSSOP-16



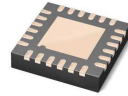
### [PCA9655EDTR2G](#)

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