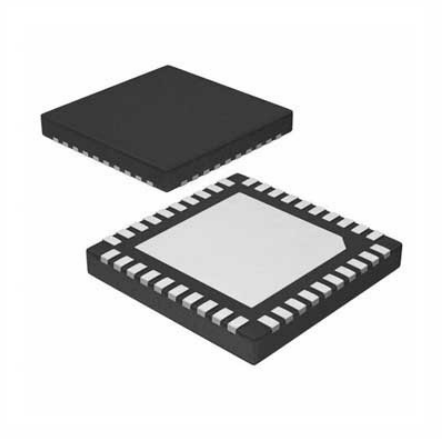
HMC1035LP6GE

Data Sheet

Clock Generator, Fractional-N Translation, 0.025 GHz to 2.5 GHz, 3.15 V to 3.5 V supply, LFCSP-40

Manufacturers	Analog Devices, Inc
Package/Case	QFN-40
Product Type	Clock & Timer ICs
RoHS	Green
Lifecycle	



Images are for reference only

Please submit RFQ for HMC1035LP6GE or Email to us: sales@ovaga.com We will contact you in 12 hours. RFQ

General Description

The HMC1035LP6GE is a low-noise, wide-band 3.3 V clock generator IC with a fractional-N Phase Locked Loop (PLL) that features an integrated Voltage Controlled Oscillator (VCO). The device provides differential clock outputs between 25 MHz and 2500 MHz range. The HMC1035LP6GE features a low noise Phase Detector (PD) and Delta-Sigma modulator, capable of operating at up to 100 MHz which permits wider loop-bandwidths and excellent spurious performance.

The HMC1035LP6GE features industry leading phase noise and jitter performance, across the operating range, that enable it to improve link level jitter performance, Bit-Error-Rates (BER) and eye diagram metrics. The superior noise floor (<-162 dBc/Hz) makes the HMC1035LP6GE an ideal source for a variety of applications–such as clock references for high speed data converters, physical layer devices (PHY), serializer/deserializer (SER DES) circuits, FPGAs and processors. The HMC1035LP6GE can also be used as an LO for 10G/40G/100G optical modules and transponders, as well as primary reference clock for 10G/40G/100G line cards, and for jitter attenuation and frequency translation.

The differential output of the HMC1035LP6GE can be set to either External Termination, which could be used for LVPECL operation, or Internal Termination for operation in an LVDS compatible mode or LVPECL. Additionally, an ouput swing adjustment makes the device flexible and compatible with a wide variety of signal level requirements. The output can be internally terminated to reduce component count and cost or could be terminated externally using standard LVPECL termination methods. An Output Mute function allows the user to shut off the outputs, such as may be required for board testing or debugging. The LVPECL/LVDS, amplitude select and Output Mute function are all programmed SPI serial programming.

The HMC1035LP6GE is designed to select between a Power Priority or a Performance Priority mode. The Power Priority setting reduces the current consumption of the part, whereas the Performance Priority setting improves the Jitter and Phase Noise performance.

The 24 bit Delta-Sigma Modulator further enhances Hittite's Exact Frequency Mode, which enables users to generate output frequencies with 0 Hz frequency error in many applications.

Features

3.3 V Only, Single Supply Rail Operation

Output Frequency Range: 25 MHz - 2500 MHz

Integer or Fractional-N mode Frequency Translation

Configurable LVDS-compatible or LVPECL type Differential Outputs

Adjustable PLL Loop BW via External Filter

Output Disable/Mute Control

Lock Detect Signal

Exact Frequency Mode to achieve reference frequency tuning, and 0 Hz frequency error

40 Lead 6x6mm SMT Package: 36mm²

Application

10G/40G/100G Optical Modules, Transponders, Line Cards

OTN and SONET /SDH Applications

Data Converters, Sample Clock Generation

Cellular/4G Infrastructure

High Frequency Processor/FPGA Clocks

Any Frequency Clock Rate Generation

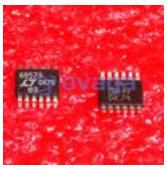
Low Jitter SAW Oscillator Replacement

DDS Replacement

Frequency Translation

Frequency Margining

Related Products



LTC6957HMS-3#PBF

Analog Devices, Inc

MSOP-12

HMC769LP6CE

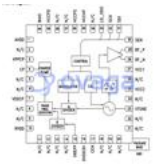
Analog Devices, Inc

40-QFN

HMC987LP5E

Analog Devices, Inc

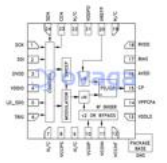
32-VFQFN



HMC838LP6CE

Analog Devices, Inc

QFN-40



HMC703LP4E

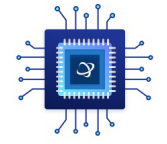
Analog Devices, Inc

QFN-24

HMC807LP6CETR

Analog Devices, Inc

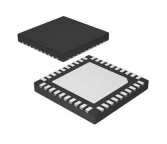
QFN40



HMC1031MS8E

Analog Devices, Inc

8-MS8E



HMC835LP6GE

Analog Devices, Inc

QFN40