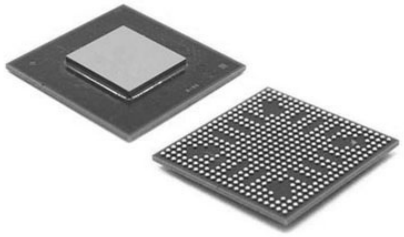
AD9653BCPZ-125

Data Sheet

Analog to Digital Converters - ADC Quad 16-Bit 125 MSPS Serial LVDS 1.8V

Manufacturers	Analog Devices, Inc
Package/Case	LFCSP-48 EP
Product Type	Data Conversion ICs
RoHS	Rohs
Lifecycle	



Images are for reference only

Please submit RFQ for AD9653BCPZ-125 or Email to us: sales@ovaga.com We will contact you in 12 hours. RFQ

General Description

The AD9653 is a quad, 16-bit, 125 MSPS analog-to-digital converter(ADC) with an on-chip sample-and-hold circuitdesigned for low cost, low power, small size, and ease of use.The product operates at a conversion rate of up to 125 MSPSand is optimized for outstanding dynamic performance and lowpower in applications where a small package size is critical.

The ADC requires a single 1.8 V power supply and LVPECL-/CMOS-/LVDS-compatible sample rate clock for full performanceoperation. No external reference or driver components arerequired for many applications.

The ADC automatically multiplies the sample rate clock for theappropriate LVDS serial data rate. A data clock output (DCO) forcapturing data on the output and a frame clock output (FCO)for signaling a new output byte are provided. Individual-channelpower-down is supported and typically consumes less than 2 mWwhen all channels are disabled. The ADC contains several featuresdesigned to maximize flexibility and minimize system cost, such as programmable output clock and data alignment and digitaltest pattern generation. The available digital test patternsinclude built-in deterministic and pseudorandom patterns, alongwith custom user-defined test patterns entered via the serial portinterface (SPI).

The AD9653 is available in a RoHS-compliant, 48-lead LFCSP.It is specified over the industrial temperature range of −40°C to+85°C.

PRODUCT HIGHLIGHTS

Small Footprint. Four ADCs are contained in a small, space-saving package.

Low power of 163 mW/channel at 125 MSPS with scalable power options.

Pin compatible to the AD9253 14-bit quad and AD9633 12-bit quad ADC.

Ease of Use. A data clock output (DCO) operates at frequencies of up to 500 MHz and supports double data rate (DDR) operation.

User Flexibility. The SPI control offers a wide range of flexible features to meet specific system requirements

Features

1.8 V supply operation

Low power: 164 mW per channel at 125 MSPS with scalable power = ±3.5 LSB (typical)

Serial LVDS (ANSI-644, default) and low power, reduced signal option (similar to IEEE 1596.3)

650 MHz full power analog bandwidth

2 V p-p input voltage range (supports up to 2.6 V p-p)

See data sheet for additional features

Application

Medical ultrasound and MRI

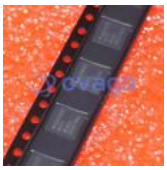
High speed imaging

Quadrature radio receivers

Diversity radio receivers

Test equipment

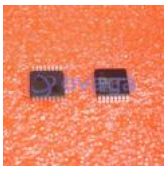
Related Products



ADAS3022BCPZ

Analog Devices, Inc

LFCSP-40



AD7266BSUZ

Analog Devices, Inc

TQPF-32

AD574AJNZ

Analog Devices, Inc

PDIP-28

AD7401YRWZ

Analog Devices, Inc

SOIC-16

AD7938BSUZ

Analog Devices, Inc

TQFP-32

AD7192BRUZ-REEL

Analog Devices, Inc

TSSOP-24

AD7124-8BCPZ-RL7

Analog Devices, Inc

LFCSP-32

AD9680BCPZ-500

Analog Devices, Inc

LFCSP-64