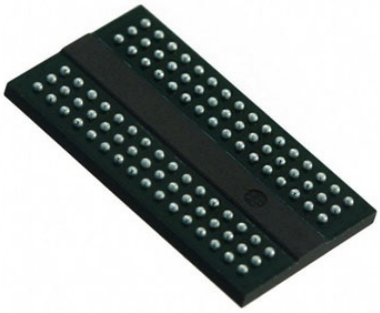
AD9689BBPZ-2000

Data Sheet

IC ADC 14BIT PIPELINED 196BGA-ED

Manufacturers	Analog Devices, Inc
Package/Case	196-LFBGA
Product Type	Data Conversion ICs
RoHS	Pb-free Halide free
Lifecycle	



Images are for reference only

Please submit RFQ for AD9689BBPZ-2000 or Email to us: sales@ovaga.com We will contact you in 12 hours. RFQ

General Description

The AD9689 is a dual, 14-bit, 2.0 GSPS/2.6 GSPS analog-to-digital converter (ADC). The device has an on-chip buffer and a sample-and-hold circuit designed for low power, small size, and ease of use. This product is designed to support communications applications capable of direct sampling wide bandwidth analog signals of up to 5 GHz. The −3 dB bandwidth of the ADC input is 9 GHz. The AD9689 is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power in a small package.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. The analog input and clock signals are differential inputs. The ADC data outputs are internally connected to four digital downconverters (DDCs) through a crossbar mux. Each DDC consists of multiple cascaded signal processing stages: a 48-bit frequency translator (numerically controlled oscillator (NCO)), and decimation rates. The NCO has the option to select preset bands over the general-purpose input/output (GPIO) pins, which enables the selection of up to three bands. Operation of the AD9689 between the DDC modes is selectable via SPI-programmable profiles.

In addition to the DDC blocks, the AD9689 has several functions that simplify the automatic gain control (AGC) function in a communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect control bits in Register 0x0245 of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input. In addition to the fast detect outputs, the AD9689 also offers signal monitoring capability. The signal monitoring block provides additional information about the signal being digitized by the ADC.

The user can configure the Subclasss 1 JESD204B-based high speed serialized output in a variety of one-lane, two-lane, four-lane, and eight-lane configurations, depending on the DDC configuration and the acceptable lane rate of the receiving logic device. Multidevice synchronization is supported through the SYSREF± and SYNCINB± input pins.

The AD9689 has flexible power-down options that allow significant power savings when desired. All of these features can be programmed using a 3-wire serial port interface (SPI).

The AD9689 is available in a Pb-free, 196-ball BGA, specified over the −40°C to +85°C ambient temperature range. This product is protected by a U.S. patent.

Note that throughout this data sheet, multifunction pins, such as FD_A/GPIO_A0, are referred to either by the entire pin name or by a single function of the pin, for example, FD_A, when only that function is relevant.

Product Highlights

Applications

Wide, input −3 dB bandwidth of 9 GHz supports direct radio frequency (RF) sampling of signals up to about 5 GHz.

Four integrated, wideband decimation filters and NCO blocks supporting multiband receivers.

Fast NCO switching enabled through the GPIO pins.

SPI controls various product features and functions to meet specific system requirements.

Programmable fast overrange detection and signal monitoring.

On-chip temperature diode for system thermal management.

12 mm × 12 mm, 196-ball BGA.

Pin, package, feature, and memory map compatible with the AD9208 14-bit, 3.0 GSPS, JESD204B dual ADC.

Features

JESD204B (Subclass 1) coded serial digital outputs

Support for lane rates up to 16 Gbps per lane

Noise density

1.55 W total power per channel at 2.56 GSPS (default settings)

SFDR at 2.56 GSPS encode

73 dBFS at 1.8 GHz A

IN

59 dBFS at 5.53 GHz A

IN

full-scale>

SNR at 2.56 GSPS encode

59.7 dBFS at 1.8 GHz A

IN

53.0 dBFS at 5.53 GHz A

IN

full-scale>

SFDR at 2.0 GSPS encode

Application

Diversity multiband and multimode digital receivers

3G/4G, TD-SCDMA, W-CDMA, and GSM, LTE, LTE-A

Electronic test and measurement systems

Phased array radar and electronic warfare

DOCSIS 3.0 CMTS upstream receive paths

HFC digital reverse path receivers

78 dBFS at 900 MHz A

IN

62 dBFS at 5.53 GHz A

IN

full-scale>

SNR at 2.0 GSPS encode

62.7 dBFS at 900 MHz A

IN

53.1 dBFS at 5.5 GHz A

IN

full-scale>

0.975 V, 1.9 V, and 2.5 V dc supply operation

9 GHz analog input full power bandwidth (−3 dB)

Amplitude detect bits for efficient AGC implementation

Programmable FIR filters for analog channel loss equalization

2 integrated, wideband digital processors per channel

48-bit NCO

Programmable decimation rates

Phase coherent NCO switching

Up to 4 channels available

Serial port control

Supports 100 MHz SPI writes and 50 MHz SPI reads

Integer clock with divide by 2 and divide by 4 options

Flexible JESD204B lane configurations

On-chip dither

Support for lane rates up to 16 Gbps per lane

73 dBFS at 1.8 GHz A

IN

59 dBFS at 5.53 GHz A

IN

full-scale>

full-scale>

59.7 dBFS at 1.8 GHz A

IN

53.0 dBFS at 5.53 GHz A

IN

full-scale>

full-scale>

78 dBFS at 900 MHz A

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62 dBFS at 5.53 GHz A

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full-scale>

full-scale>

62.7 dBFS at 900 MHz A

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53.1 dBFS at 5.5 GHz A

IN

full-scale>

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48-bit NCO

Programmable decimation rates

Up to 4 channels available

Supports 100 MHz SPI writes and 50 MHz SPI reads

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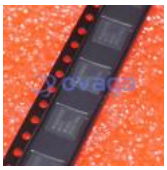
Related Products



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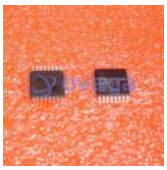
Analog Devices, Inc

LFCSP-40



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TQPF-32

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LFCSP-64