

DAC 1-CH Resistor-String 12-bit 6-Pin SC-70 T/R

Manufacturers	Analog Devices, Inc
Package/Case	SC70-6
Product Type	Data Conversion ICs
RoHS	Rohs
Lifecycle	



Images are for reference only

Please submit RFQ for AD5621AKSZ-REEL7 or [Email to us: sales@ovaga.com](mailto:sales@ovaga.com) We will contact you in 12 hours.

[RFQ](#)

General Description

The AD5601/AD5611/AD5621, members of the nanoDAC® family, are single, 8-/10-/12-bit, buffered voltage output DACs that operate from a single 2.7 V to 5.5 V supply, consuming typically 75 μ A at 5 V. The parts come in tiny LFCSP and SC70 packages. Their on-chip precision output amplifier allows rail-to-rail output swing to be achieved. The AD5601/AD5611/AD5621 utilize a versatile 3-wire serial interface that operates at clock rates up to 30 MHz and is compatible with SPI, QSPI™, MICROWIRE™, and DSP interface standards.

The reference for the AD5601/AD5611/AD5621 is derived from the power supply inputs and, therefore, gives the widest dynamic output range. The parts incorporate a power-on reset circuit, which ensures that the DAC output powers up to 0 V and remains there until a valid write to the device takes place.

The AD5601/AD5611/AD5621 contain a power-down feature that reduces current consumption to typically 0.2 μ A at 3 V.

They also provide software-selectable output loads while in power-down mode. The parts are put into power-down mode over the serial interface.

The low power consumption of these parts in normal operation makes them ideally suited to portable battery-operated equipment. The combination of small package and low power makes these nanoDAC devices ideal for level-setting requirements, such as generating bias or control voltages in space-constrained and power-sensitive applications.

Product Highlights

Available in 6-lead LFCSP and SC70 packages.

Low power, single-supply operation. The AD5601/AD5611/AD5621 operate from a single 2.7 V to 5.5 V supply with a maximum current consumption of 100 μ A, making them ideal for battery-powered applications.

The on-chip output buffer amplifier allows the output of the DAC to swing rail-to-rail with a typical slew rate of 0.5 V/ μ s.

Reference is derived from the power supply.

High speed serial interface with clock speeds up to 30 MHz. Designed for very low power consumption. The interface powers up only during a write cycle.

Power-down capability. When powered down, the DAC typically consumes 0.2 μ A at 3 V. Power-on reset with brownout detection.

Features

6-lead SC70 and LFCSP packages

Micropower operation: 100 μ A maximum at 5 V

Power-down typically to 0.2 μ A at 3 V

2.7 V to 5.5 V power supply

Guaranteed monotonic by design

Power-on reset to 0 V with brownout detection

3 power-down functions

Low power serial interface with Schmitt-triggered inputs

On-chip output buffer amplifier, rail-to-rail operation

SYNC interrupt facility

Minimized zero-code error

AD5601 buffered 8-bit DAC

B version: ± 0.5 LSB INL

AD5611 buffered 10-bit DAC

B version: ± 0.5 LSB INL

A version: ± 4 LSB INL

AD5621 buffered 12-bit DAC

B version: ± 1 LSB INL

A version: ± 6 LSB INL

Application

Voltage level setting

Portable battery-powered instruments

Digital gain and offset adjustment

Programmable voltage and current sources

Programmable attenuators



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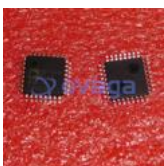
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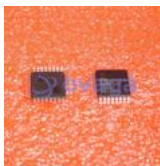
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LFCSP-64