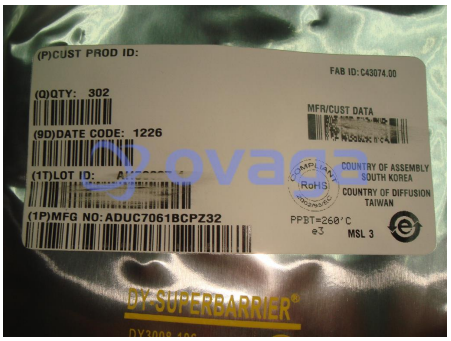
ADUC7061BCPZ32

Data Sheet

Low-Power, Precision Analog Microcontroller, Dual - ADCs, Flash/EE, ARM7TDMI; No of Pins: 32; Temperature Range: Industrial



Images are for reference only

Manufacturers	Analog Devices, Inc
Package/Case	LFCSP-32
Product Type	Embedded Processors & Controllers
RoHS	Rohs
Lifecycle	

Please submit RFQ for ADUC7061BCPZ32 or Email to us: sales@ovaga.com We will contact you in 12 hours. RFQ

General Description

The ADCs consists of a 5-channel primary ADC and up to an 8-channel auxiliary ADC. The ADCs operate in single-ended or differential input modes. A single channel buffered voltage output DAC is available on-chip. The DAC output range is programmable to one of two voltage ranges.

The devices operate from an on-chip oscillator and a PLL gene-rating an internal high frequency clock up to 10.24 MHz. The microcontroller core is an ARM7TDMI, 16-bit/32-bit RISC machine offering up to 10 MIPS peak performance. 4 kB of SRAM and 32 kB of nonvolatile Flash/EE memory are provided on-chip. The ARM7TDMI core views all memory and registers as a single linear array.

The ADuC7060/ADuC7061 contain four timers. Timer 1 is wake-up timer with the ability to bring the part out of power saving mode. Timer 2 may be configured as a watchdog timer. A 16-bit PWM with six output channels is also provided.

The ADuC7060/ADuC7061 contain an advanced interrupt controller. The vectored interrupt controller (VIC) allows every interrupt to be assigned a priority level. It also supports nested interrupts to a maximum level of eight per IRQ and FIQ. When IRQ and FIQ interrupt sources are combined, a total of 16 nested interrupt levels are supported.On-chip factory firmware supports in-circuit serial download via the UART serial interface ports and nonintrusive emulation via the JTAG interface.

The parts operate from 2.375 V to 2.625 V over an industrial temperature range of −40°C to +125°C.

Features

Analog input/output - See data sheet for additional information.

MicrocontrollerARM7TDMI core, 16-/32-bit RISC architectureJTAG port supports code download and debugMultiple clocking options

Memory32 kB (16 kB × 16) Flash/EE memory4 kB (1 kB × 32) SRAM

ToolsIn-circuit download, JTAG based debugLow cost, QuickStart development system

Communications interfaces

SPI interface (5 Mbps)4-byte Rx and Tx FIFOs

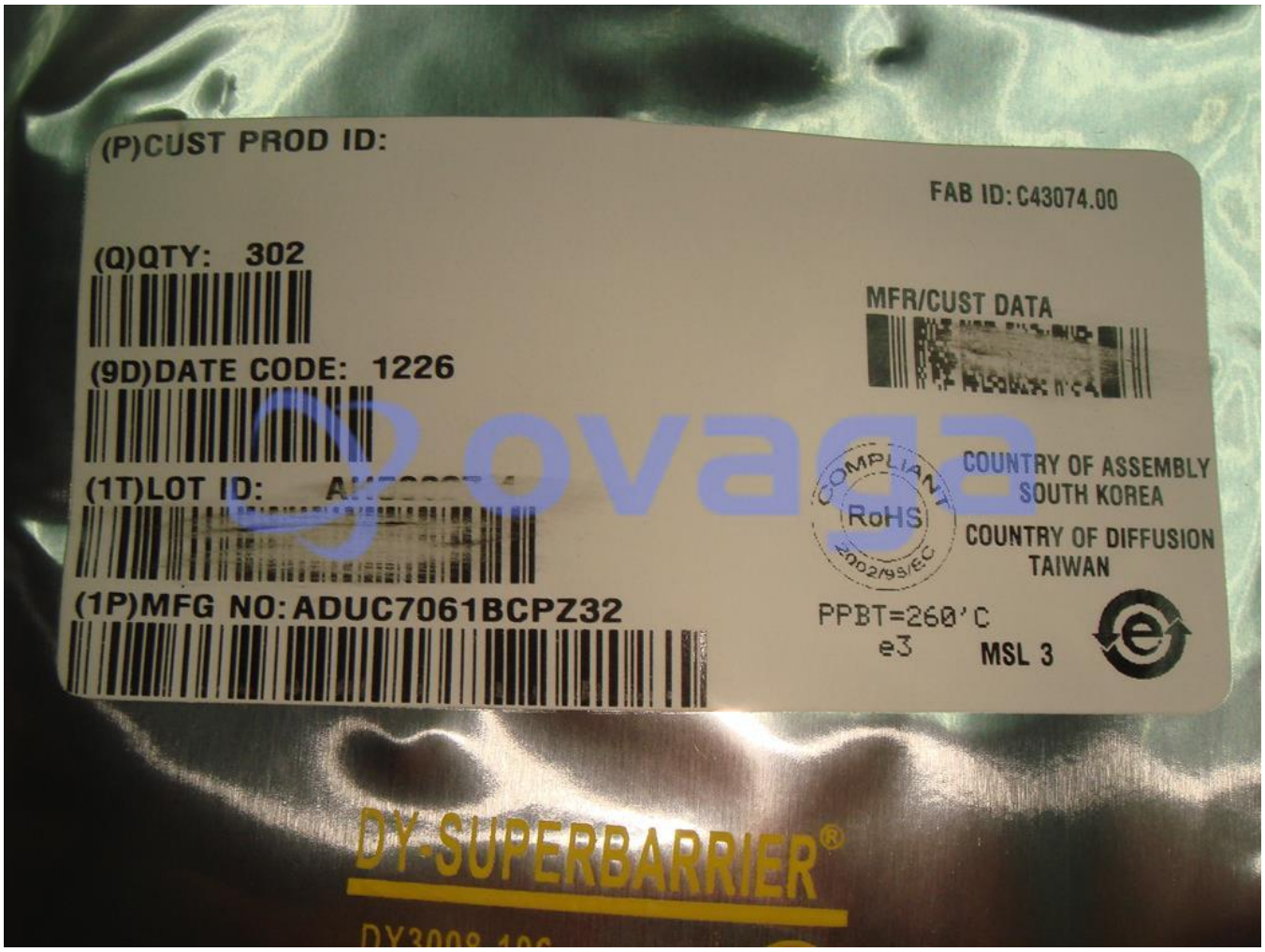
UART serial I/O and I2C (master/slave)

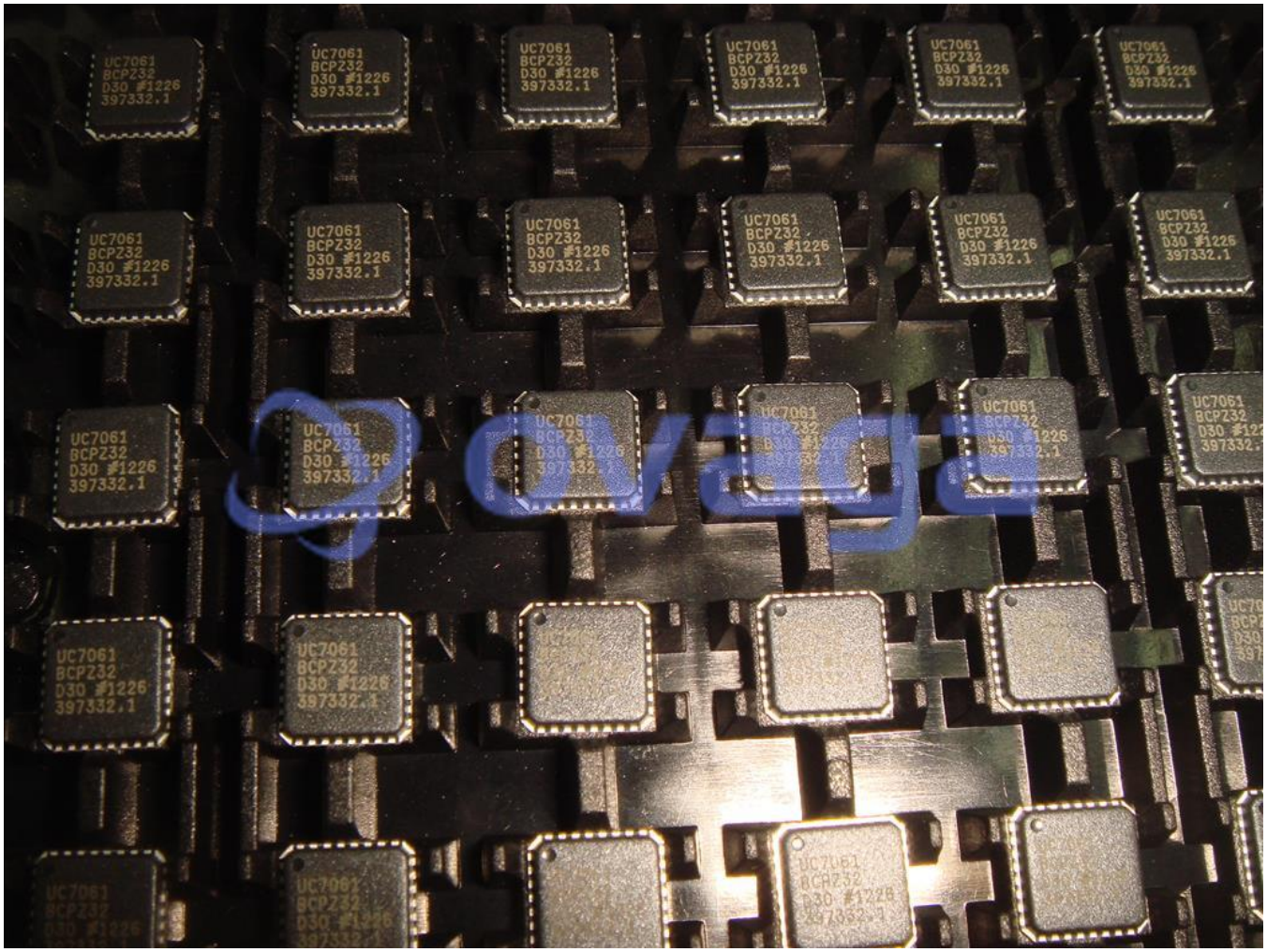
See Data Sheet for Additional Information

Application

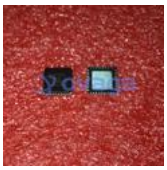
Industrial automation and process control

Intelligent, precision sensing systems, 4 mA to 20 mA loop-based smart sensors





Related Products



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LFCSP-40

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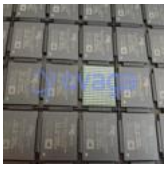

[ADSP-BF561SBBCZ-5A](#)

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CSPBGA-256